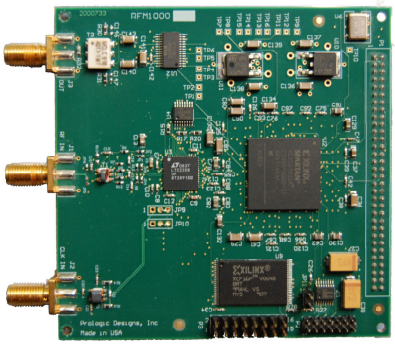
RFM1000
130 MSPS ADC/DAC/FPGA Board

Features

- **16 Bit 130 MSPS ADC (LTC2208)**
- **14 Bit 125 MSPS DAC (DAC904)**
- **Xilinx XC3SD1800A-4 FPGA**
- **On board 100MHz clock**
- **External clock input**
- **2x32 2mm interface header**
- **3.500" x 3.500"**
- **$995**
- **For complete system, see RFM1000LAN**



Overview

RFM1000 is a low cost module that adds RF signal capture and generation to your product without the headaches, cost, and risk associated with high speed ADC/DAC/FPGA design and manufacturing. A 2x32 2mm header provides access to 46 FPGA signals for easy interface to almost any electronic system.

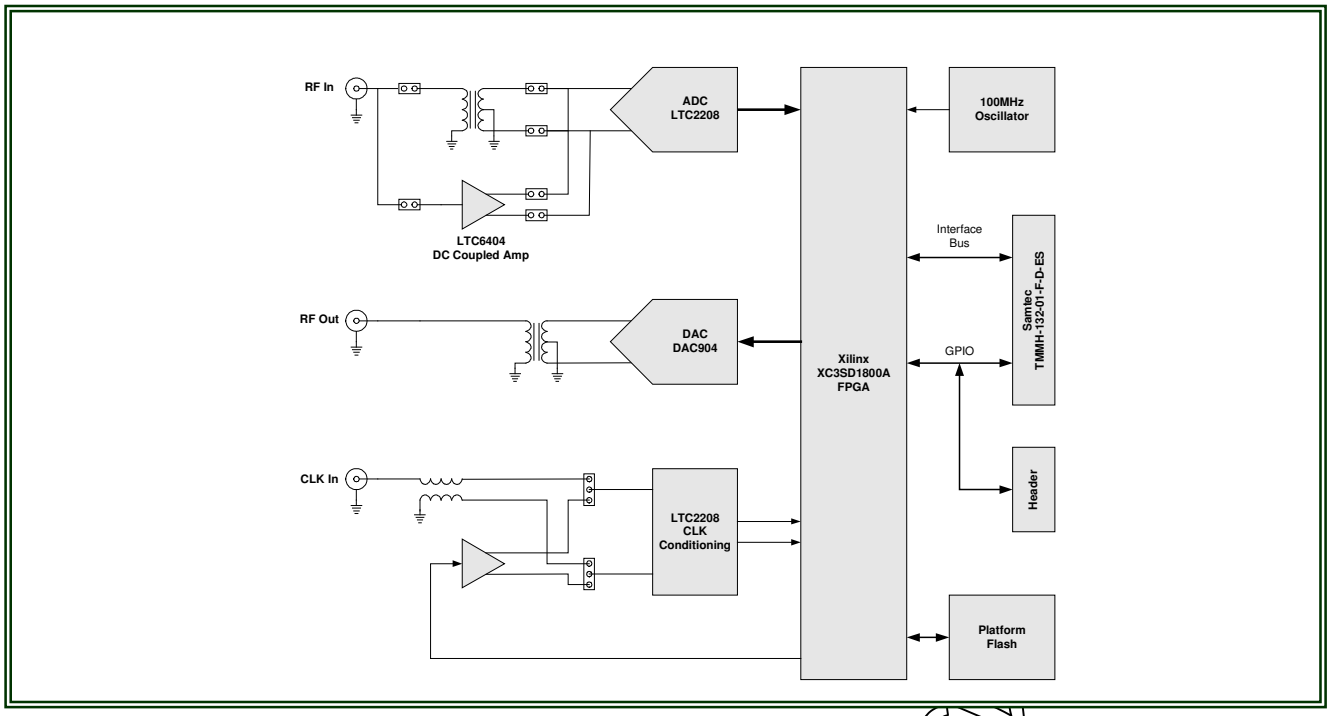
FPGA

The RFM1000 board is shipped with a default FPGA configuration that will satisfy the requirements for many applications as is. This standard off the shelf configuration provides basic ADC/DAC functionality, includes a 64K sample ADC buffer, a 16K sample DAC waveform buffer, as well as user programmable trigger sources, ADC/DAC gate delays and sample gate widths. In addition, a "DDS" mode enables the RFM1000 to be used as a high quality CW RF signal source. FPGA memory and registers are accessible via the 2x32 header signals.

Advanced users can develop and program custom FPGA configurations using Xilinx development tools. The original configuration can be restored by the user at any time. Prologic Designs can provide custom FPGA configurations. Please call to discuss your application.

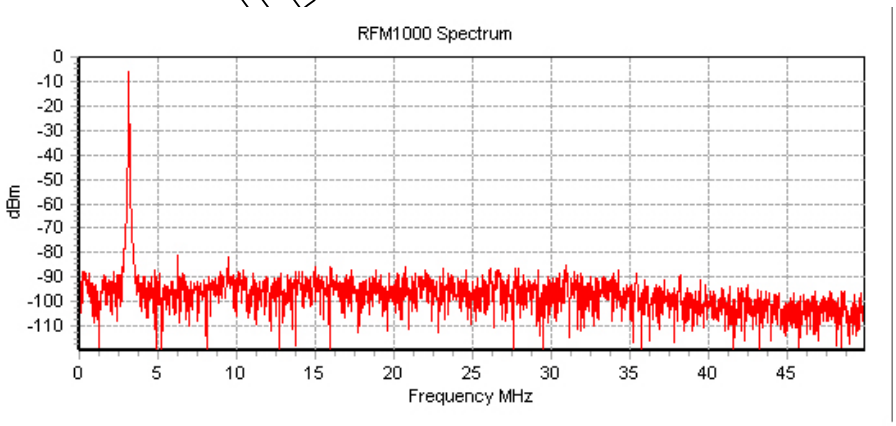
Prologic Designs, Inc
10 Gerard Ave ♦ Suite 108 ♦ Timonium, MD 21093 ♦ 410-560-3515

RFM1000 Simplified Block Diagram



Mechanical

3.500” x 3.500”
Drawing: To be released



Prologic Designs, Inc
10 Gerard Ave ♦ Suite 108 ♦ Timonium, MD 21093 ♦ 410-560-3515

Specifications

ADC	
ADC IC	Linear Technology LTC2208
Resolution	16 Bits
Conversion Clock	1 – 130 MHz
DAC	
DAC IC	Texas Instruments DAC904
DAC Resolution	14 Bits
Conversion Clock	DC-125 MHz
RF Input	
RF Input Voltage	2.2VPP
RF Input Impedance	50 Ohms
RF Input Bandwidth	50KHz – 200MHz
RF Out	
RF Output Voltage	700 mVPP into 50 Ohms, amplitude programmable
RF Output Bandwidth	400KHz – 62.5 MHz
Clock Input	
External Clock Input Impedance	50 Ohms
External Clock Signal Level	100mVPP – 1VPP, sinusoidal
Base FPGA Configuration	
Address	16 Bits, LVTTL [1]
Data	16 Bits, LVTTL [1]
GPIO	8 Bits, LVTTL [1]
Power Requirements	5V @ 500mA
Dimensions	3.500” x 3.500”

Notes:
1. FPGA Configurable

For additional information contact:

Prologic Designs Inc
10 Gerard Ave
Suite 108
Timonium, MD 21093
410-560-3515